Amendments to the Claims:

Rewrite the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. – 11 (canceled)

12. (currently amended) A memory architecture comprising:

a level one cache comprising texel information;

a level two cache, coupled to the level one cache, that comprises overlapping fetched texel information resulting from execution of previous memory fetch ~~instructions, and~~ instructions;

wherein when the level one cache does not comprise overlapping fetched texel information requested by a subsequent memory fetch instruction, the level two cache is operative to transmit the overlapping fetched texel information requested by the subsequent memory fetch instruction to the level one ~~cache.~~ cache; and

wherein each of the previous memory fetch instructions and the subsequent memory fetch instruction result in storage of requested texel information at least in the level one cache.

13. (previously presented) The memory architecture of claim 12, wherein:

the level one cache comprises a plurality of texture cache blocks; and

wherein one of the plurality of texture cache blocks is operative to receive the subsequent texel fetch instruction.

14. (previously presented) The memory architecture of claim 12, further comprising:

a main memory operatively coupled to the level two cache; and

wherein when the level one cache and the level two cache do not comprise texel information requested by a second subsequent memory fetch instruction, the main memory is operative to transmit the texel information requested by the second subsequent memory fetch instruction to the level two cache for storage.

15. (previously presented) The memory architecture of claim 14, wherein the level two cache transmits the texel information requested by the second subsequent texel fetch instruction to the level one cache for storage.

16. (currently amended) A graphics processing device, comprising:

a graphics controller operative to execute memory fetch instructions;

a main memory;

a level one cache coupled to the graphics controller, the level one cache comprising texel information; and

a level two cache coupled between the main memory and the level one cache, the level two cache comprising overlapping fetched texel information resulting from execution of previous memory fetch ~~instructions, and~~ instructions;

wherein when the level one cache does not comprise overlapping fetched texel information requested by a subsequent memory fetch instruction, the level two cache transmits the overlapping fetched texel information requested by the subsequent memory fetch instruction to the level one ~~cache.~~ cache; and

wherein each of the previous memory fetch instructions and the subsequent memory fetch instruction result in storage of requested texel information at least in the level one cache.

17. (previously presented) The graphics processing device of claim 16, wherein the graphics controller is operative to request the subsequent memory fetch instruction.

18. (previously presented) The graphics processing device of claim 17, wherein the graphics controller comprises a plurality of fetch blocks, wherein one of the plurality of fetch blocks is operative to request the subsequent memory fetch instruction.

19. (previously presented) The graphics processing device of claim 17, wherein the level one cache transmits the overlapping fetched texel information requested by the subsequent memory fetch instruction to the graphics controller.

20. (previously presented) The graphics processing device of claim 16, wherein

the level one cache comprises a plurality of texture cache blocks; and

wherein one of the plurality of texture cache blocks is operative to receive the subsequent texel fetch instruction.

21. (previously presented) The graphics processing device of claim 16, wherein when the level one cache and the level two cache do not comprise texel information requested by a second subsequent memory fetch instruction, the main memory is operative to transmit the texel information requested by the second subsequent memory fetch instruction to the level two cache for storage.

22. (previously presented) The graphics processing device of claim 21, wherein the level two cache transmits the texel information requested by the second subsequent texel fetch instruction to the level one cache for storage.